1- Application of Image Registration Techniques to Medical CT and MR Images

Abstract: Image registration has become one of the most widely used techniques in computer vision. Its applications include optical flow, motion analysis, tracking, face detection, and biomedical image registration. In the present work, three different techniques of image registration were implemented and applied to both Computed Tomography (CT) and Magnetic Resonance (MR) images. The first technique is based on Cross Correlation (CC). The second approach depends on Control Points’s Selection (CPS) from both the reference and the input images. The last technique is based on Maximization of Mutual Information (MMI) between the two images. The registrability is calculated for each image to measure its ability to provide unambiguous registration, by providing clear correlation peaks when registered with another subimage. Then, the three registration techniques were evaluated and compared using both the Weighted Peak Signal to Noise Ratio (WPSNR) and the Normalized Cross Correlation Coefficient (NCCC). The application of the selected techniques to CT and MR images has shown that registration based on MMI has given the best results and can be used efficiently for alignment of CT and MR images.

2- Application of Image Fusion Techniques for Detection of Early Hemorrhagic Transformation in Hyper-acute Ischemic Stroke

Abstract: Image fusion aims at the integration of complementary data in two or more images to enhance information apparent in these images. In the present work, three image fusion techniques were implemented; the Laplacian Pyramid, the Wavelet Transform, and the Multi-focus Technique based on Spatial Frequency. Fusion results were evaluated according to three measures of performance; the entropy, the cross entropy and the spatial frequency. Image fusion techniques were applied to facilitate detection of early hemorrhagic transformation in hyperacute ischemic stroke by fusing CT and MR images taken at the same level. The fused image had led to higher detection accuracy.

3- Detection of Head and Neck Cancer Using Image Fusion of Early and Delayed CT Scans

Abstract: In the present work, four different image fusion techniques were implemented and applied to Computed Tomography (CT) and images. These are the Laplacian Pyramid, the Wavelet Transform, the Computationally Efficient Pixel-level Image Fusion (CEMIF) method, and the Multi-focus Technique based on Spatial Frequency. Fusion results were evaluated according to three measures of performance; the entropy, the cross entropy and the spatial frequency. Image fusion techniques were applied to facilitate detection of head and neck cancer using two sets of CT images; early (30 sec delay), and delayed (180 sec delay) CT images. The fused CT image depicts combined tumor enhancement and vessel opacification. This had led to higher detection accuracy of head and neck cancer than using conventional CT images.

4- Applying Image Fusion Techniques for Detection of Hepatic Lesions
Abstract: Image fusion is the process by which two or more images are combined into a single image retaining the important features from each of the original images. It aims at the integration of complementary data to enhance the information apparent in the images as well as to increase the reliability of the interpretation. The successful fusion of images acquired from different modalities or instruments is of great importance in many applications such as medical imaging, microscopic imaging, remote sensing, computer vision, and robotics. In the present work, four different image fusion techniques were implemented and applied to Computed Tomography (CT) and Magnetic Resonance imaging (MRI). These are the Laplacian Pyramid, the Wavelet Transform, the Computationally Efficient Pixel-level Image Fusion (CEMIF) method, and the Multi-focus Technique based on Spatial Frequency. Fusion results were evaluated according to three measures of performance; the entropy, the cross entropy and the spatial frequency. Image fusion techniques were applied to facilitate detection of hepatic lesions by fusing MRI and CT images at the same level. The fused images had led to higher detection accuracy than using either CT or MR images.

5-
**An ANN Majority Logic Gate (MLG) Using Single Electron Nano-Devices**

The Single Electron Nano-Devices (SENDs) are attractive candidates for post-CMOS VLSI era mainly due to its very low power consumption. In this paper, the Linear Threshold Gate (LTG) SEND is reviewed. An Artificial Neural Network (ANN) Majority Logic Gate (MLG) with 3 inputs (MLG3) is proposed. The MLGs with different inputs (from 3 to 7) are implemented using LTG and SET inverter SENDs. The detailed parameters for all used devices as well as the corresponding SIMON 2.0 simulation results of these MLGs are included.

6-
**The Implementation of 2-Bit Decoders Using Single Electron Linear Threshold Gates**

The Single Electron (SE) Linear Threshold Gate (LTG) is one of the basic functional Single Electron Nano-Devices (SENDs). In this paper, a proposed 2-bit decoder that is composed of only four LTGs is presented. Both active-HIGH and active-LOW SE LTG 2-bit decoders are proposed. The detailed schematic diagrams along with the corresponding simulation results (using SIMON 2.0) of these 2-bit decoders are included.

7-
**A Single Electron ANN Majority Logic Gate**

The Single Electron Nano-Devices (SENDs) are attractive candidates for post-CMOS VLSI era mainly due to its very low power consumption. In this paper, the Linear Threshold Gate (LTG) SEND is reviewed. An Artificial Neural Network (ANN) Majority Logic Gate (MLG) with 3 inputs (MLG3) is proposed. The MLGs with three and four inputs are implemented using LTG and SET inverter SENDs. The detailed parameters for all used devices as well as the corresponding SIMON 2.0 simulation results of these MLGs are included.

8-
**Analysis of Semiconductor Electronics Circuits Using an Interactive e-Learning Package at Mansoura University**
An interactive e-learning package is being developed at Mansoura University (MU) to help electronics engineering students better understand the basics of the semiconductor electronics devices (i.e., diodes and transistors). The developed package includes three main modules. The first module is an illustrative one that explains the characteristics of the electronics devices using different educational techniques including interactive animations. The second module contains a circuit analyzer program that can be used to analyze electronics circuits composed of these semiconductor devices. The analyzer produces the voltages at all circuit nodes and the currents in all circuit branches. The third module is an interactive oscilloscope that displays the signals at any circuit node.

9-

**The Design of Logic Gates Using Single Electron Box (SEB) Nano-Devices**

The Single Electron Box (SEB) is the basic functional Single Electron Nano-Devices (SENDs). In this paper, a detailed analysis of the SEB basic operation is reviewed. The SEB with extra input capacitors is presented with adjusted parameters so as to get same digital levels for both inputs and outputs. Both NOT and NAND logic gates followed by a double-inverter stage are proposed. The detailed schematic diagrams along with the corresponding simulation results (using SIMON 2.0) of these SEB logic gates are included.

10-

**Rough Set Analysis and Cloud Model Algorithm to Automated Knowledge for Classification IRIS to Achieve High Security**

Most of Intrusion Detection Systems uses all data features to detect an intrusion. Very little work addresses the importance of having a small feature subset in designing an efficient intrusion detection system. Some features are redundant and some contribute little to the intrusion detection process. Purpose of this study is to investigate the effectiveness of Rough Set Theory in identifying the important features in building an Intrusion detection system. Rough Set is also used to classify Iris data. Here, we used CASIA V1.0 (CASIAIrisV1) data, presents In this paper, a new algorithm, Decision Tree Construction based on Rough Set Theory under Characteristic Relation (DTCRSCR), is proposed for mining classification knowledge from incomplete information systems. The algorithm is then used in iris classification. Its idea is to select the attribute whose weighted mean roughness under the characteristic relation as current splitting node. Our framework RST- DTCRSCR method result has a higher accuracy as compared to either full feature or entropy.

11-

**Design and Simulation of a Universal N-Bit Binary Encoder Using Single Electron Linear Threshold Gates**

The Single-Electron (SE) Linear Threshold Gate (LTG) is one of the basic functional Single-Electron Nano-Devices (SENDs). In this paper, using a SE LTG as the basic
building block in an artificial neural network (ANN) is reviewed. A universal SE ANN 2-bit (4-to-2) binary encoder, which is composed of only two SE LTGs, is designed. The detailed schematic diagrams along with the corresponding SIMON 2.0 simulation results (that include input and output signals as well as the stability diagrams) of the designed binary encoder are included. The proposed SE ANN 2-bit binary encoder can easily be generalized to design n-bit binary encoders. As an example of this generalization, a SE ANN 3-bit (8-to-3) binary encoder, which is composed of three SE LTGs, is designed and its SIMON 2 simulation results are presented. This design is compared with the previously reported C_SET 3-bit binary encoder.

12-

**A 3-Input Universal Logic Gate (ULG) Using a Single Electron Linear Threshold Gate**

The Single Electron NanoDevices (SENDs) are attractive candidates for post-CMOS VLSI era mainly due to its very low power consumption. In this paper, the Single Electron (SE) Linear Threshold Gate (LTG) is reviewed. A 3-input Universal Logic Gate (ULG) is proposed. The universality of this gate is demonstrated by showing how to achieve all possible 8 combinations of output logic functions. This is presented by using two versions of the ULG3; i.e., NEG-ULG3 and POS-ULG3. The detailed parameters for all used devices as well as the corresponding SIMON 2.0 simulation results are included.

13-

**Design and Simulation of Single-Source Single-Electron Complementary 4-Bit Multiplexing Nano-Circuits**

The Single-Electron Transistor (SET) and Linear Threshold Gate (LTG) are among the basic functional Single-Electron Nano-Devices (SENDs). In this paper, these basic SENDs are used to design a single-source (SS) single-electron (SE) complementary 4-bit (4-to-1) multiplexer. This design is compared with the previously reported multiple-source SE complementary 4-bit multiplexer. The first reported SS SE complementary 4-bit demultiplexer is also introduced. The detailed schematic diagrams as well as the corresponding simulation results of the designed SE 4-bit multiplexer/demultiplexer (using SIMON 2.0 and SECS Monte Carlo (MC) SE simulators) are illustrated. The simulation results include input, control, and output signals; free energy and stability diagrams; and maximum allowed signal frequency. The estimated delay and energy consumption is calculated and presented.

14-

**Design and Simulation of Novel Single-Electron Coding Nano-Circuits Using Room Temperature Summing-Inverter Gates**

The Single-Electron (SE) summing-inverter (SI) NOR and NAND gates are among the basic functional SE circuits. In this paper, the design of multi-input SE SI NOR and NAND gates are reviewed. Novel SE decimal-to-BCD encoders and binary decoders, which are composed of SI gates, are designed for all combinations of active inputs and outputs. The simulated designs work properly with only one voltage source of 500 mV for a wide range of temperatures (from 40K to 400K). The detailed schematic diagrams along with the corresponding SIMON 2 simulation results at room temperature (that include input and output signals as well as the stability diagrams) of the novel SE
decimal-to-BCD encoders as well as the developed SE binary decoders are presented.

15-

**Performance Measures for Image Fusion Based on Wavelet Transform and Curvelet Transform**

Curvelet transform is a recently-developed multi-scale transforms, which is more suitable for objects with curves. Applications of the curvelet transform have increased rapidly in the field of image fusion. Image fusion means the combining of two images into a single image that has the maximum information content without producing details that are nonexistent in the given images. In the present work an algorithm for image fusion based on the curvelet transform was implemented, analyzed, and compared with a wavelet-based fusion algorithm. Two famous applications of image fusion are introduced: fusion of multi-focus images and fusion of multi-exposure images. Fusion results were evaluated and compared according to three measures of performance; the entropy (H), the mutual information (MI) and the amount of edge information (QAB/F). The three quantitative performance measures have shown that the curvelet based image fusion algorithm provides a slightly better fused image than the wavelet algorithm. In addition, the fused image has a better eye perception than the input ones.

16-

**Single-Electron 2-Bit Decoders Using Room-Temperature Summing-Inverter Gates**

The Single-Electron (SE) summing-inverter (SI) logic gates are among the basic functional SE circuits. In this paper, the design of SE SI NAND and NOR gates is reviewed. Two SE SI 2-bit decoders were designed and simulated for the cases of active-LOW and active-HIGH outputs. The simulated designs work properly with only one voltage source of 500 mV for a wide range of temperatures (from 40K to 400K). The detailed schematic diagrams along with the corresponding SIMON 2.0 simulation results at room temperature (that include input and output signals as well as the stability diagrams) for both cases of the developed SE SI 2-bit decoders are presented.

17-

**Optimized Single-Electron NAND-Based D-Latch / Flip-Flop**

The single-electron (SE) linear threshold gate (LTG) and the CMOS-based single-electron transistor (SET) inverter are among the basic functional Single-Electron Nano-Devices (SENDs). In this paper, the SE implementation of n-input buffered NAND gates, each consists of a SE LTG AND gate followed by a CMOS-based SET inverter, is reviewed. Two optimized SE NAND-based sequential digital basic building blocks are designed and simulated using the Monte Carlo (MC) Nano-simulator SIMON 2.0. These basic building blocks are the D-latch and the positive-edge-triggered (PET) D flip-flop with asynchronous Preset and Clear. The estimated delay and energy consumption of these circuits are calculated and presented. Sequential digital circuits can be implemented using the developed optimized SE NAND-based PET D flip-flops.

18-

**Analysis and Classification of Sleep EEG**

In the present paper, a comparative study of performance for three techniques of feature extraction is presented in order to classify the sleep stages using EEG signals. A multilayer feed forward neural network was used for classification. Six sleep EEG
records for each of ten patients were selected from Cairo Center of Sleep Disorder. Three methodologies of analysis were utilized for feature extraction. These include: autoregressive modeling (AR), bispectral analysis, and discrete wavelet transform (DWT), where principle component analysis (PCA) was used to reduce feature dimensionality. The features derived from the three methodologies of signal analysis were used as input feature vectors to the classifier. Information fusion is very important task in pattern recognition as it is difficult to develop classifiers with a high identification performance rate. The multilayer feed forward neural network gives higher classification rate using the data fusion at the feature extraction level. It reaches 83.4%.